

AMENDMENTS TO THE CLAIMS

Claims 1 through 11. (Cancelled).

12. (Currently Amended) A semiconductor device comprising:

a dielectric layer formed over a conductive feature having an upper surface;

an opening in the dielectric layer over the upper surface of the conductive feature features;

a silicon carbide layer having [[a]] an upper silicon surface region lining the opening;

a diffusion barrier layer on the silicon surface region of the silicon carbide layer and in contact with the upper surface of the conductive feature; and

copper (Cu) or Cu alloy filling the opening.

13. (Original) The semiconductor device according to claim 12, wherein:

the dielectric layer comprises a first dielectric layer, a middle etch stop layer on the first dielectric layer and a second dielectric on the middle etch stop layer; and

the opening is a dual damascene opening comprising a lower via second in the first dielectric layer and an upper trench section in the second dielectric layer.

14. (Original) The semiconductor device according to claim 13, wherein each of the first and second dielectric layers comprises a dielectric material having a dielectric constant (k) no greater than 3.9.

15. (Original) The semiconductor device according to claim 14, wherein each of the first and second dielectric layers comprises a dielectric material having a porosity of 10% to 20%.

16. (Original) The semiconductor device according to claim 13, wherein the thickness of the silicon carbide layer with the silicon surface region is 30 Å to 90 Å.

17. (Original) The semiconductor device according to claim 16, wherein the silicon surface region has a thickness of 10 Å to 20 Å.

18. (Original) The semiconductor device according to claim 13, wherein the barrier layer comprises tantalum, tantalum nitride, or a composite comprising a layer of tantalum nitride on the silicon carbide layer and a layer of tantalum on the layer of tantalum nitride.

19. (Original) The semiconductor device according to claim 14, wherein the silicon carbide layer having the silicon surface region has a combined thickness of 30 Å to 90 Å.

20. (Currently Amended) The semiconductor device according to claim 19, wherein the silicon rich silicon surface region has a thickness of 10 Å to 20 Å.